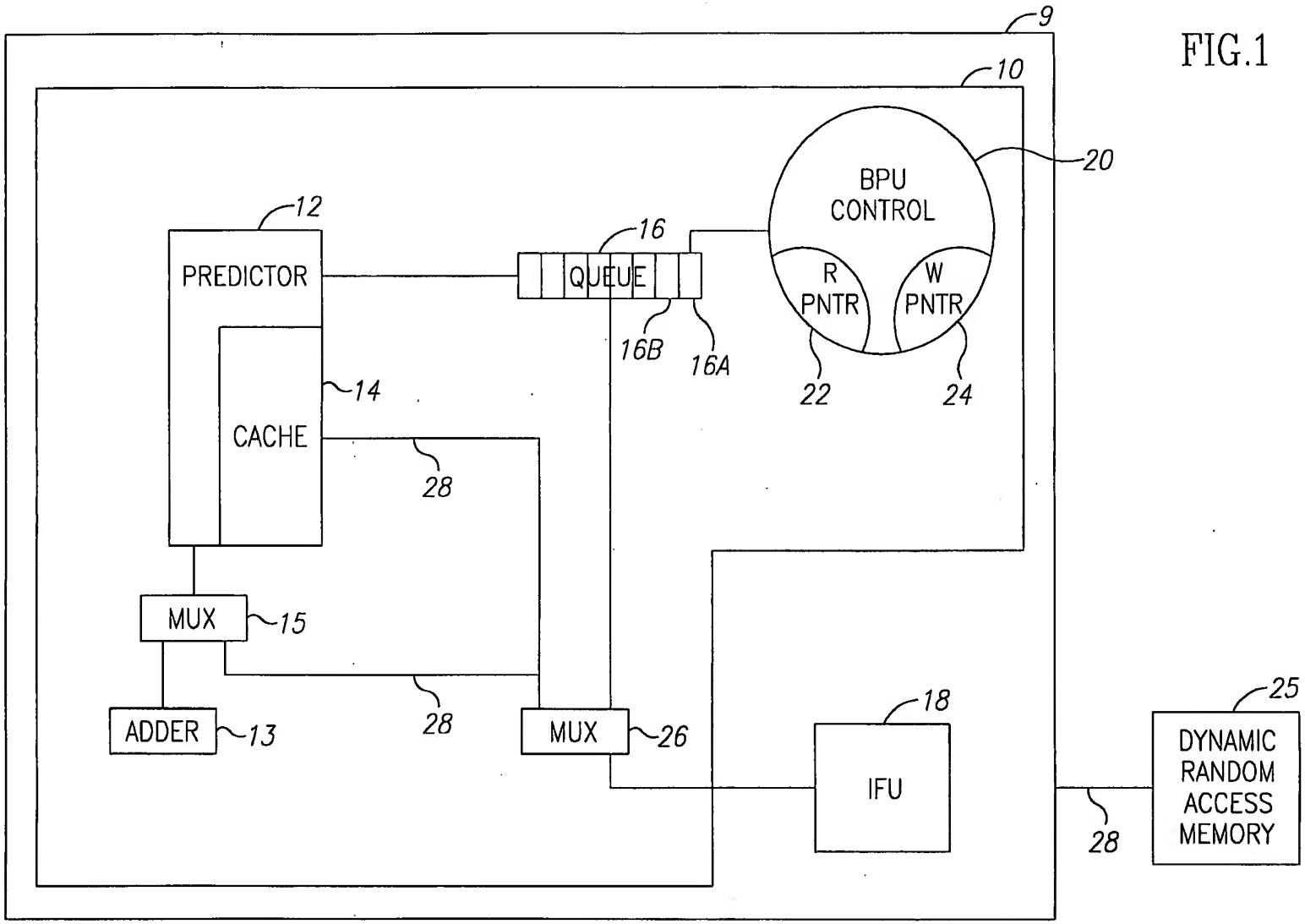
9
10
20
BPU
CONTROL
12
PREDICTOR
16
QUEUE
R
PNTR
W
PNTR
16B
16A
22
24
14
CACHE
28
MUX
15
ADDER
13
28
MUX
26
18
IFU
25
DYNAMIC
RANDOM
ACCESS
MEMORY
28

FIG.1

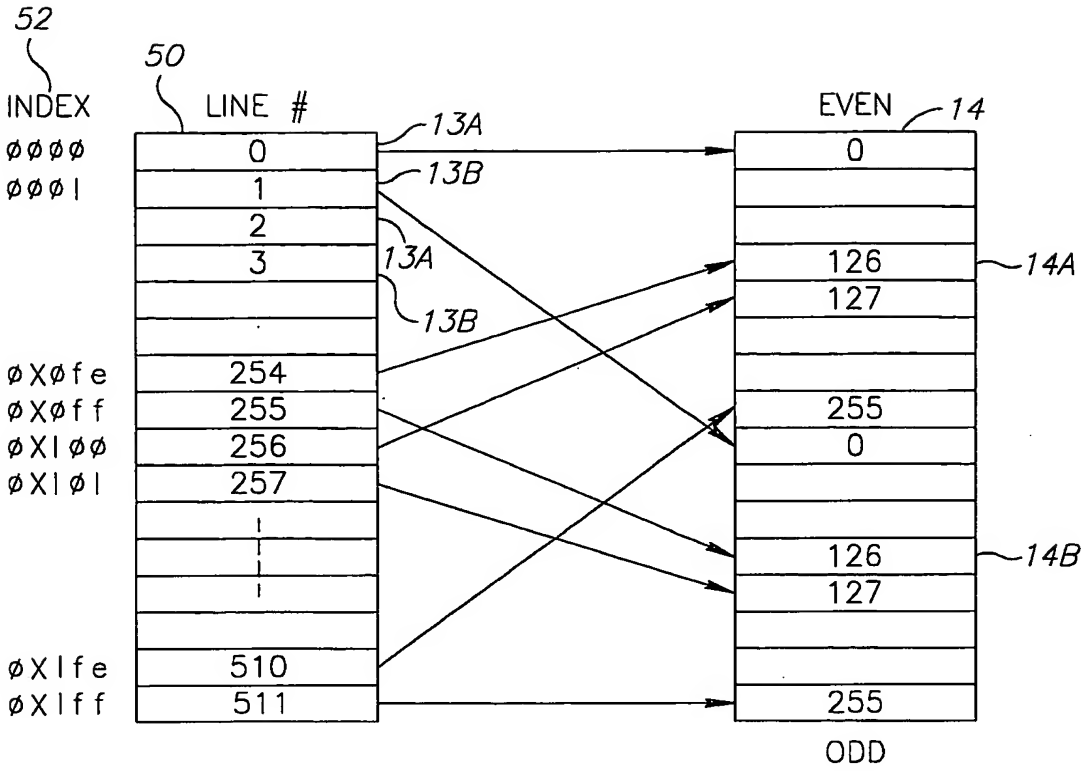
52
50
INDEX
LINE #
EVEN
14
13A
13B
13A
13B
14A
14B
ØØØØ
ØØØ1
ØX0fe
ØX0ff
ØX1ØØ
ØX1Ø1
ØX1fe
ØX1ff
0
1
2
3
254
255
256
257
510
511
0
126
127
255
0
126
127
255
ODD

FIG.2

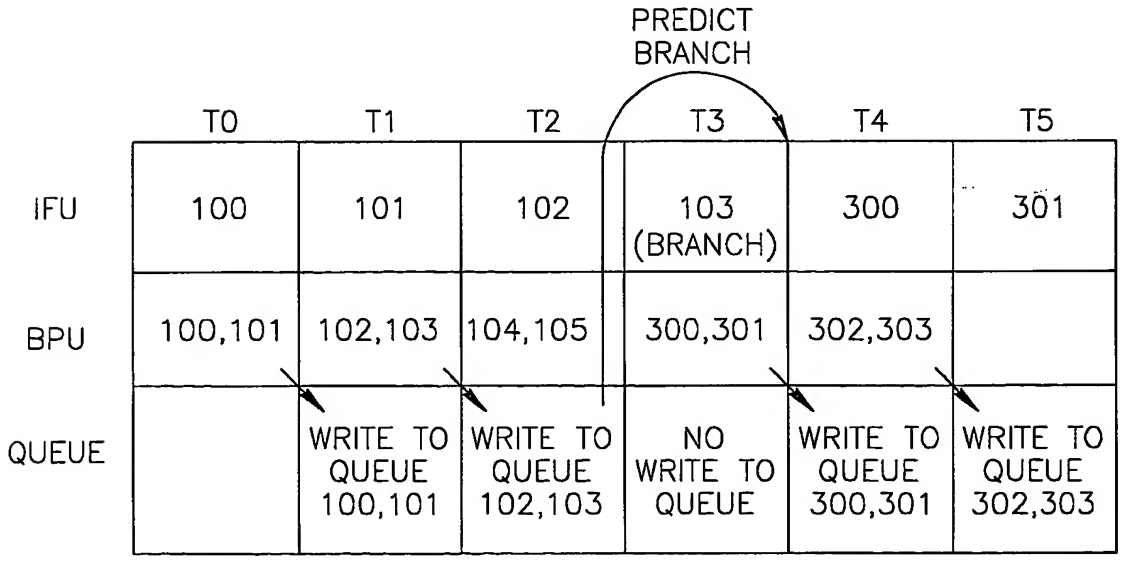
PREDICT BRANCH
T0
T1
T2
T3
T4
T5
IFU
100
101
102
103 (BRANCH)
300
301
BPU
100,101
102,103
104,105
300,301
302,303
QUEUE
WRITE TO QUEUE 100,101
WRITE TO QUEUE 102,103
NO WRITE TO QUEUE
WRITE TO QUEUE 300,301
WRITE TO QUEUE 302,303

FIG.3

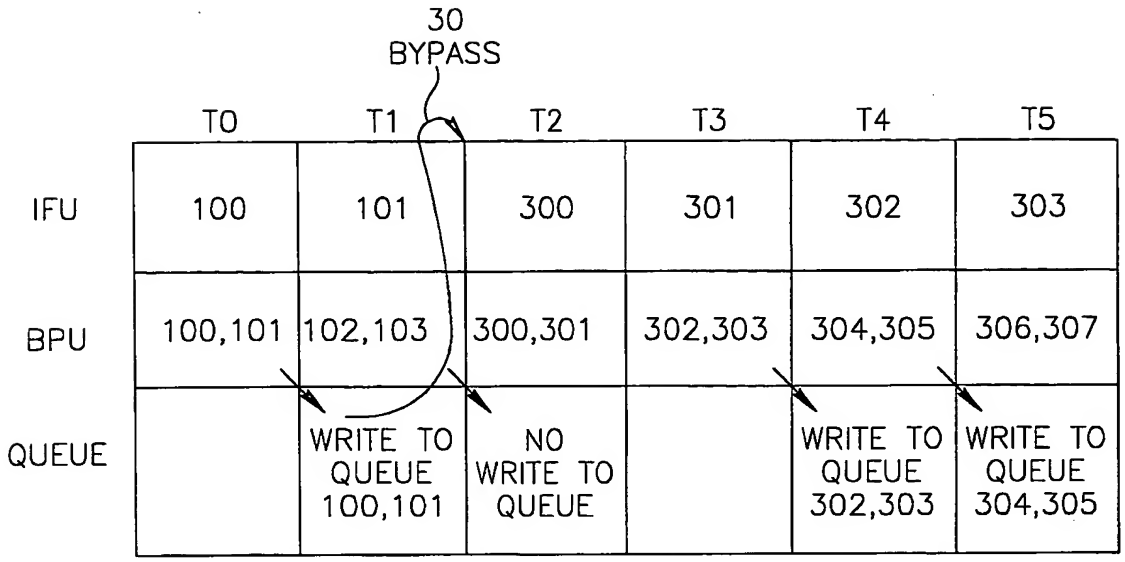
30
BYPASS
T0
T1
T2
T3
T4
T5
IFU
100
101
300
301
302
303
BPU
100,101
102,103
300,301
302,303
304,305
306,307
QUEUE
WRITE TO QUEUE 100,101
NO WRITE TO QUEUE
WRITE TO QUEUE 302,303
WRITE TO QUEUE 304,305

FIG.4

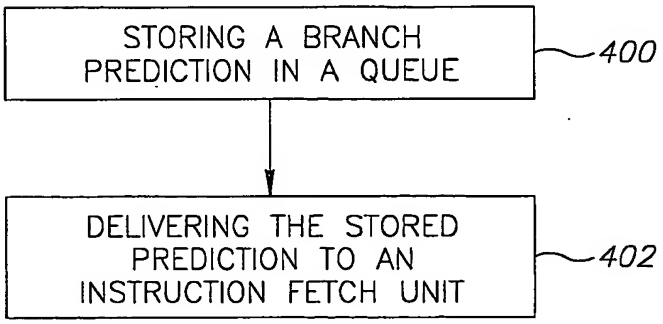
STORING A BRANCH PREDICTION IN A QUEUE
400
DELIVERING THE STORED PREDICTION TO AN INSTRUCTION FETCH UNIT
402

FIG.5